

Refine Search

Search Results -

Terms	Documents
L2 and switch	425

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<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L3</u>	L2 and switch	425	<u>L3</u>
<u>L2</u>	L1 same memory same cache	808	<u>L2</u>
<u>L1</u>	((disk or disc) near5 controller) same interface	9740	<u>L1</u>

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L3	0

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<u>L4</u>	L3	0	<u>L4</u>
	<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L3</u>	L2 and switch	425	<u>L3</u>
<u>L2</u>	L1 same memory same cache	808	<u>L2</u>
<u>L1</u>	((disk or disc) near5 controller) same interface	9740	<u>L1</u>

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/229 709/232 709/253 710/313 710/316 710/104 710/74 710/1 710/305 711/112 711/113 711/114 711/147 711/148 711/130 714/3 714/7).ccls.	13526

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L5</u> 710/313,316,104,74,1,305;711/112-114,147,148,130;714/3,7;709/229,232,253.ccls.	13526	<u>L5</u>
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L4</u> <u>L3</u>	0	<u>L4</u>
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L3</u> L2 and switch	425	<u>L3</u>
<u>L2</u> L1 same memory same cache	808	<u>L2</u>
<u>L1</u> ((disk or disc) near5 controller) same interface	9740	<u>L1</u>

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L6 and (request near5 computer)	77

Database:

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 Derwent World Patents Index
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Search:

L8

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L8 L6 and (request near5 computer)

77 L8

L7 L6 and computer

170 L7

L6 l3 and L5

172 L6

L5 710/313,316,104,74,1,305;711/112-114,147,148,130;714/3,7;709/229,232,253.ccls.

13526 L5

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L3

0 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L2 and switch

425 L3

L2 L1 same memory same cache

808 L2

L1 ((disk or disc) near5 controller) same interface

9740 L1

END OF SEARCH HISTORY



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» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

Modify Search

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Multiprocessor cache analysis using ATUM

Sites: R.L. Agarwal, A.
Digital Equipment Corp., Hudson, MA, USA;

This paper appears in: **Computer Architecture, 1988. Conference Proceedings. 15th Annual International Symposium on**

Publication Date: 30 May-2 June 1988

On page(s): 186 - 195

Meeting Date: 05/30/1988 - 06/02/1988

Location: Honolulu, HI

INSPEC Accession Number: 3228434

DOI: 10.1109/ISCA.1988.5228

Posted online: 2002-08-06 15:52:23.0

Abstract

A tracing facility called ATUM-2 that allows the capture of large address traces of multiprocessors is described. The method is based on a previous scheme called address tracing using microcode (ATUM) for single processors (see *ibid.*, vol.13, p.119-27, (1986)). In ATUM, the microcode of a machine is modified to record the address of the **memory** references as a side effect of normal execution. The addresses are recorded in a reserved portion of main **memory**, and periodically transferred to disk. The ATUM-2 implementation on a VAX 8350 multiprocessor is described and the use of the resulting traces to analyze physical versus virtual addressing of large **caches**, process-identifier hashing in virtual **caches**, **cache** interference between multiple processes, **cache** interference between multiple CPUs, process affinity, and semaphore usage in writeback **caches** is reported on

Index Terms

Inspec

Controlled Indexing

computer architecture multiprocessors systems storage allocation storage management

Non-controlled Indexing

ATUM-2 VAX 8350 multiprocessor address tracing using microcode **cache interference** **memory references** multiprocessor **cache analysis** process affinity process-identifier hashing tracing facility

Author Keywords

Not Available

References

No references available on IEEE Xplore.

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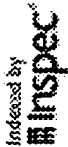
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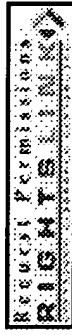
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Cost-efficient memory architecture design of NAND flash memory embedded systems

Park, C., Seo, J., Seo, D., Kim, S., Kim, B.
SAMSUNG Electronics Co., Ltd.

This paper appears in: **Computer Design, 2003. Proceedings. 21st International Conference on**

Publication Date: 13-15 Oct. 2003

On page(s): 474 - 480

Number of Pages: xii+563

ISSN: 1063-6404

INSPEC Accession Number: 7946671

DOI: 10.1109/ICCD.2003.1240943

Posted online: 2003-10-27 09:54:46.0

Abstract

NAND flash memory has become an indispensable component in embedded systems because of its versatile features such as nonvolatility, solid-state reliability, low cost and high density. Even though NAND flash memory gains popularity as data storage, it also can be exploited as code memory for XIP (execute-in-place). We present a cost-efficient memory architecture, which incorporates NAND flash memory into an existing memory hierarchy for code execution. The usefulness of the proposed approach is demonstrated with real embedded workloads on a real hardware prototyping board.

Index Terms

Index

Controlled Indexing

NAND circuits cache storage embedded systems flash memories logic design memory architecture memory expansion boards

Non-controlled Indexing

NAND flash memory XIP code memory cost-efficient memory architecture design embedded systems execute-in-place memory hierarchy real hardware prototyping board

Author Keywords

Not Available

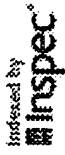
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L8: Entry 1 of 77

File: PGPB

Jul 7, 2005

PGPUB-DOCUMENT-NUMBER: 20050149688
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050149688 A1

TITLE: Computer system and a method of assigning a storage device to a computer

PUBLICATION-DATE: July 7, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kitamura, Manabu	Yokohama	CA	JP	
Yamagami, Kenji	Los Gatos		US	
Murakami, Tatsuya	Odawara		JP	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	COUNTRY	TYPE CODE
Hitachi, Ltd.				03

APPL-NO: 11/ 072723 [\[PALM\]](#)

DATE FILED: March 7, 2005

RELATED-US-APPL-DATA:

Application 11/072723 is a continuation-of US application 10/095582, filed March 13, 2002, PENDING

Application 10/095582 is a continuation-of US application 09/642817, filed August 22, 2000, US Patent No. 6854034

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
JP	11-241024	1999JP-11-241024	August 27, 1999

INT-CL: [07] [G06](#) [F](#) [12/00](#)US-CL-PUBLISHED: [711/170](#); [711/112](#), [711/114](#), [711/113](#)US-CL-CURRENT: [711/170](#); [711/112](#), [711/113](#), [711/114](#)

REPRESENTATIVE-FIGURES: 4

ABSTRACT:

A computer system which has a plurality of computers and a storage device subsystem connected to the plurality of computers. The storage device subsystem has a plurality of storage devices and a plurality of interfaces, through which the subsystem is connected to the computers. One of the plurality of computers has a management means for holding therein data indicative of the storage devices and a connection relationship between the computers and storage device subsystem. Each computer, when wanting a new device, informs the management means of its capacity and type. The management means receives its notification and selects one of the storage devices which satisfies the request. And the management means instructs the storage device subsystem to set predetermined data in such a manner that the computer can access the

selected device. The management means also returns predetermined data to the computer as a device assignment requester, the assignment requester computer modifies setting thereof to allow the computer in question can use the assigned device.

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L8: Entry 5 of 77

File: PGPB

Jul 7, 2005

PGPUB-DOCUMENT-NUMBER: 20050149671
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050149671 A1

TITLE: Disk array apparatus and method for controlling the same

PUBLICATION-DATE: July 7, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Suzuki, Katsuyoshi	Odawara		JP	
Hirasawa, Akihisa	Odawara		JP	

APPL-NO: 11/ 056002 [\[PALM\]](#)
DATE FILED: February 14, 2005

RELATED-US-APPL-DATA:

Application 11/056002 is a continuation-of US application 10/659398, filed September 11, 2003,
PENDING

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
JP	2003-145111	2003JP-2003-145111	May 22, 2003

INT-CL: [07] [G06 F 12/00](#)

US-CL-PUBLISHED: 711/114

US-CL-CURRENT: [711/114](#)

REPRESENTATIVE-FIGURES: 12

ABSTRACT:

An apparatus includes a controller and a plurality of disk drives. The controller has a communication control unit for accepting a data input/output request, a disk controller unit for controlling a disk drive, and a cache memory for temporarily storing data transferred between the communication control unit and the disk controller unit. The plurality of disk drives has different communication interfaces and connected to the disk controller unit to communicate with the disk controller unit.

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is a continuation of application Ser. No. 10/659,398, filed Sep. 11, 2003 and is related to Japanese Patent Application No. 2003-145111, filed on May 22, 2003, the contents of which are incorporated herein by reference in its entirety.

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L8: Entry 41 of 77

File: USPT

Jun 21, 2005

US-PAT-NO: 6910102

DOCUMENT-IDENTIFIER: US 6910102 B2

TITLE: Disk storage system including a switch

DATE-ISSUED: June 21, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsunami; Naoto	Sagamihara			JP
Oeda; Takashi	Sagamihara			JP
Yamamoto; Akira	Sagamihara			JP
Mimatsu; Yasuyuki	Fujisawa			JP
Sato; Masahiko	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 10/ 769922 [PALM]

DATE FILED: February 3, 2004

PARENT-CASE:

This is a continuation application of U.S. Ser. No. 10/405,645, filed on Apr. 3, 2003 now U.S. Pat. No. 6,851,029, which is a continuation application of U.S. Ser. No. 10/095,581, filed Mar. 13, 2002, now U.S. Pat. No. 6,701,411, which is a continuation application of U.S. Ser. No. 09/468,327, filed on Dec. 21, 1999, now U.S. Pat. No. 6,542,961. This application is related to U.S. Ser. No. 10/095,578, filed Mar. 13, 2002.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-364079	December 22, 1998

INT-CL: [07] G06F01200

US-CL-ISSUED: 711/114; 711/112, 711/130, 711/161, 711/162, 711/170, 714/6, 710/10, 709/220, 709/221, 709/222

US-CL-CURRENT: 711/114; 709/220, 709/221, 709/222, 710/10, 711/112, 711/130, 711/161, 711/162, 711/170, 714/6

FIELD-OF-SEARCH: 711/114, 711/112, 711/130, 711/161, 711/162, 711/170, 714/6, 710/10, 709/220, 709/223, 709/222

PRIOR-ART-DISCLOSED:

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> 5140592	August 1992	Idelman et al.	714/5
<input type="checkbox"/> 5237658	August 1993	Walker et al.	710/38
<input type="checkbox"/> 5257391	October 1993	DuLac et al.	710/10
<input type="checkbox"/> 5423046	June 1995	Nunnelley et al.	711/114
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ART-UNIT: 2186

PRIMARY-EXAMINER: Elmore; Stephen

ATTY-AGENT-FIRM: Mattingly, Stanger, Malur & Brundidge, P.C.

ABSTRACT:

A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switch connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

32 Claims, 30 Drawing figures

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File: USPT

Nov 11, 2003

US-PAT-NO: 6647461

DOCUMENT-IDENTIFIER: US 6647461 B2

TITLE: Disk array controller, its disk array control unit, and increase method of the unit

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fujimoto; Kazuhisa	Kokubunji			JP
Kanai; Hiroki	Higashiyamoto			JP
Fujibayashi; Akira	Kokubunji			JP
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APPL-NO: 10/ 335899 [\[PALM\]](#)

DATE FILED: January 3, 2003

PARENT-CASE:

The present application is a continuation of application Ser. No. 10/234,471, filed Sep. 5, 2002; now U.S. Pat. No. 6,519,680 which is a continuation of application Ser. No. 09/663,379, filed Sep. 15, 2000, now U.S. Pat. No. 6,477,619, the contents of which are incorporated herein by reference.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2000-072469	March 10, 2000

INT-CL: [07] [G06 F 12/02](#)

US-CL-ISSUED: 711/114; 711/113, 711/148, 710/313, 710/316

US-CL-CURRENT: [711/114](#); [710/313](#), [710/316](#), [711/113](#), [711/148](#)

FIELD-OF-SEARCH: 711/113, 711/114, 711/148, 710/313, 710/316

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

[Search Selected](#)[Search ALL](#)[Clear](#)

PAT-NO

ISSUE-DATE

PATENTEE-NAME

US-CL

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
1166693	March 1999	JP	

ART-UNIT: 2187

PRIMARY-EXAMINER: Nguyen; Hiep T.

ATTY-AGENT-FIRM: Antonelli, Terry, Stout & Kraus, LLP

ABSTRACT:

A disk array controller is made up of multiple disk array control units for implementing the data read/write operation and each having channel IF units, disk IF units, cache memory units and shared memory units. The disk array controller further includes inter connections for interconnecting the shared memory units and interconnecting the cache memory units across the border of disk array control units. Thereby alleviating the deterioration of performance due to the data transfer between the disk array control units, when the multiple disk array control units are to be operated as a single disk array controller.

8 Claims, 22 Drawing figures

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